Remarks:

Applicant thanks the examiner for pointing out the areas where the claims were non-compliant with 37CFR 1.121(a)(2)(ii).

Pursuant to the Notice of non-compliant Amendment mailed March 29, 2007 applicant has made the necessary amendments to claims 2 and 3.

For purposes of convenience the rest of the Remarks in the response to the Office Action previously presented are repeated below.

Claim Rejections – 35 USC 112

Claim 2 was rejected under the second paragraph of 35 USC 112 as being unclear regarding which p+ and n+ regions are referred to when saying the p+ region is on the high voltage side of the n+ region.

It is respectfully pointed out the claim defines a forward biased diode under normal operation and it is the p and n material of this diode that is being referred to. In particular the claim defines an LVTSCR which has existing p+ and n+ regions in the p-well and in accordance with the invention, at least one additional p+ and at least one additional n+ region are formed in the p-well. Thus there are multiple p+ regions and multiple n+ regions in the p-well that can define a diode in accordance with the invention. Specifically, the diode of the invention is a diode between any one of these p+ regions in the p-well (which together with the p-well forms the p-portion of the diode) and any one of the n+ regions in the p-well.

Furthermore, the LVTSCR under normal operation has the n+ and p+ regions in the n-well defining an input node or anode or high voltage node (see discussion on page 2, lines 20-28) and a the n+ and p+ regions in the p-well defining the output node or cathode or low voltage node. Thus the high voltage side under normal operation is on the n-well side and the low voltage side is on the p-well side. This SCR/LVTSCR operation is fully described on page 2, line 27 to page , line 18 and is well known in the art. Therefore voltage will always decrease from the input node on the n-well side to the output node at the p-well side. Therefore claiming the p+ region of the diode to be on the high voltage side simply means that it has to be nearer to

the n-well. This is also shown in Figure 4 and the anode and cathode of the diodes are described on page 9, lines 1-4.

Claim 2 has also been amended to explicitly state that the forward biased diode can be between any n+ region and any p+ region in the p-well. Also the n+ and p+ regions in the n-well have been defined as the high voltage node, while the n+ and p+ regions in the p-well have been defined as the low voltage node to avoid any confusion or ambiguity about what is meant by the high voltage side.

Claim Rejections – 35 USC 103

Claims 2-4 were rejected over Ker in view of Yu

The present invention claims a structure that has the features of an LVTSCR (see claim 2 which requires "LVTSCR structure that includes an n-well and a p-well formed in a substrate, an n+ region and a p+ region formed in the n-well to define a high voltage node and an n+ region and a p+ region formed in the p-well to define a low voltage node". In addition, the invention provides for adding at least one n+ region and at least one p+ region to the p-well to define a **forward biased p-n junction under normal operation**.
Under normal operation a higher voltage will be applied to the high voltage node on the n-well side while the low voltage node on the p-well side will be at a lower voltage. The claim is therefore clear that the structure needs multiple p+ regions and multiple n+ regions in the p-well.

Ker clearly lacks such multiple n+ regions and multiple p+ regions in the p-well.

Yu also lacks such multiple n+ regions and multiple p+ regions in a p-well. Furthermore Yu does not define a p-n junction that is forward biased under normal operation. Instead, in Yu the p+ region 56 is connected to ground or Vss while the n+ region 50 is on the high voltage Vcc side. Thus the diode is reverse biased (n+ region 50 on the high voltage side) under normal operation. This is also described in Yu at column 5, lines 34-38 which speaks of the diode formed from regions 50, 56 being forward biased only when the I/O pad 14 has a negative input.

In contrast, when there is excess forward bias of the pad 14, the p+ diffusion 28 and n+ diffusion 34 act as diode, which are both located in the n-well, not the p-well. Thus there is no forward biased diode in the p-well under normal operation.

Thus neither of the cited references taken alone or together disclose or suggest multiple n+ regions and multiple p+ regions in a p-well. Also, neither of the references discloses or suggests a forward biased diode in a p-well under normal operation.

In view of the differences of the cited art applicant requests that the case be allowed. As mentioned in the original response, this case has gone through numerous refilings and an appeal that was withdrawn. **To avoid further delays in having the case allowed applicant requests an interview with the examiner and his supervisor to discuss the present invention and any concerns the examiner may have. Please advise applicant by phone at 917-348 9936 or by email at jvollrath2000@yahoo.com if there is a preferred date and time for an interview with the examiner and his supervisor. The examiner has indicated that he attempted to contact the applicant on 12/22/06 for which applicant thanks the examiner and apologizes for any inconvenience caused thereby. Please note that applicant's phone number has changed but the email address remains the same. If there is no preferred date and time applicant will phone the examiner to arrange an interview.**

Respectfully Submitted,

Dated: 4/25/, 2007

Jurgen K. Vollrath

VOLLRATH & ASSOCIATES
588 Sutter Street #531, San Francisco, CA, 94102
Telephone: (917)348 9936